Examples of 1 PPS Clock Measuring Systems

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Introduction

This paper describes design, setup and use of two simple 1 PPS clock measuring systems. In these systems, digital logic divides the two sources being compared down to 1 PPS and their time difference is measured with a high resolution time interval counter, as shown in the block diagram of Figure 1.

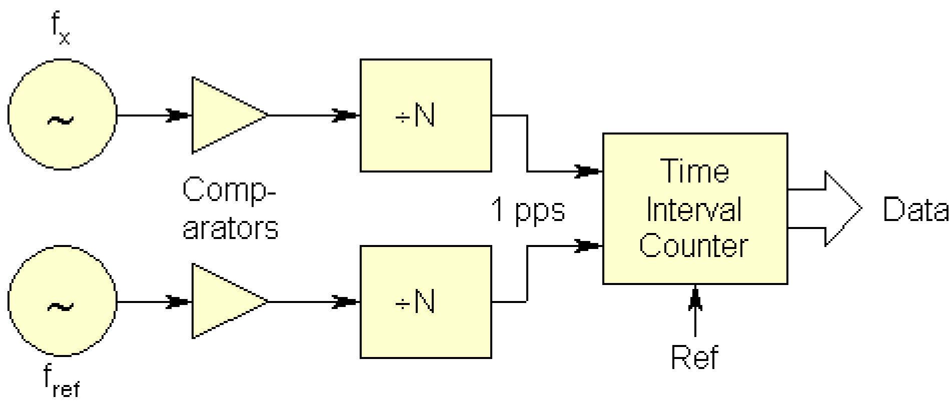

Figure 1. 1 PPS Time Interval Counter Clock Measuring System

This measurement method is made practical by modern high-resolution interpolating time interval counters that offer 9-digit/second or greater resolution. The resolution is not affected by the division ratio, which sets the minimum measurement time, and, along with the frequency offset, determines how long data can be taken before experiencing a phase spillover (which can be hard to remove from a data set). For example, a source having a frequency offset of $1\text{x}10^{-6}$ can be measured for only about 5.8 days before experiencing a 1 PPS phase spillover after being initially set at the center.

Hardware Description

The experimental 1 PPS divider hardware comprises two divider assemblies and a high resolution time interval counter. The dividers, devised by Tom Van Baak, employ PIC microcontrollers, produce a number of output rates, and include provisions for synchronization to an external 1 PPS reference. A photograph of a breadboard of the 1 PPS dividers is shown in Figure 2. See Reference [1] below for more information about these dividers.

For this test, one 10 MHz input channel was driven from a small ovenized crystal oscillator and the other from a commercial rubidium frequency reference.

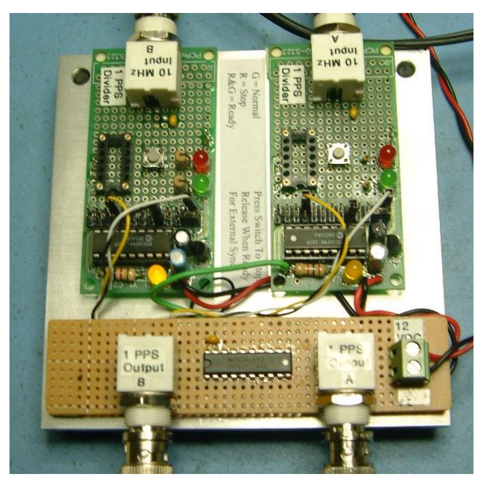

Figure 2. 1 PPS Dividers

The two 1 PPS outputs were connected to a Racal Dana 1992 time internal counter having 1 nanosecond resolution, and the start and stop signals were separated sufficiently in time for the counter to function properly.

● Interface

A Prologix GPIB-USB Controller (see Figure 2) provides a simple, low-cost interface from the counter's GPIB port to a computer's USB port [2]. The computer acquires, formats and saves the frequency data with the EZGPIB program [4], and the resulting data are analyzed with Stable32 [5]. The EZGPIB program has functions to strip off non-numeric characters from the counter's data stream, to insert MJD timetags and to store the resulting data to a Stable32-compatible disk file.

Figure 2. Prologix GPIB-USB Controller

● Measurements

Measurements were made with this setup for about one day.

● Analysis

The resulting time tagged 1-second phase data were read into Stable32. Because of the large (≈ -3.17 ppm) frequency offset of the crystal oscillator, the phase record is essentially a straight line with a large negative slope representing the frequency offset as shown in Figure 3.

Next, the phase data were converted to frequency data as shown in Figures 4 and 5. These values are obviously highly-quantized because of the 1 ns resolution of the time interval counter, as seen even more clearly in the histogram of Figure 6. This quantization causes a noise level of 1/√12 or about 0.3 ns (3x10-10 at 1-second).

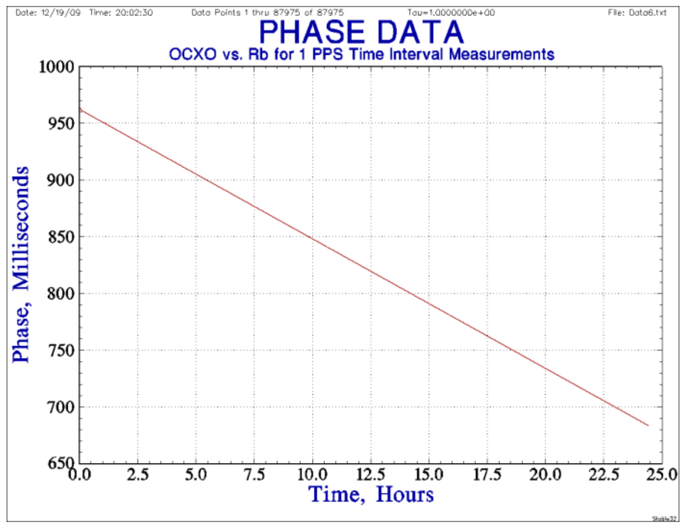

Figure 3. Phase Data Plot

The resulting frequency stability, shown in Figure 7, is white PM quantization noise out to an averaging time of about 100 seconds. The measured 1-second ADEV of about $1x10^{-9}$ thus barely reflects the instability of the small OCXO. Clearly, this system has insufficient resolution to measure the short-term stability of a good crystal oscillator. It would, however, be adequate for making a 1PPS comparison against a GPS receiver where the short-term noise is on the order of 10 nsec.

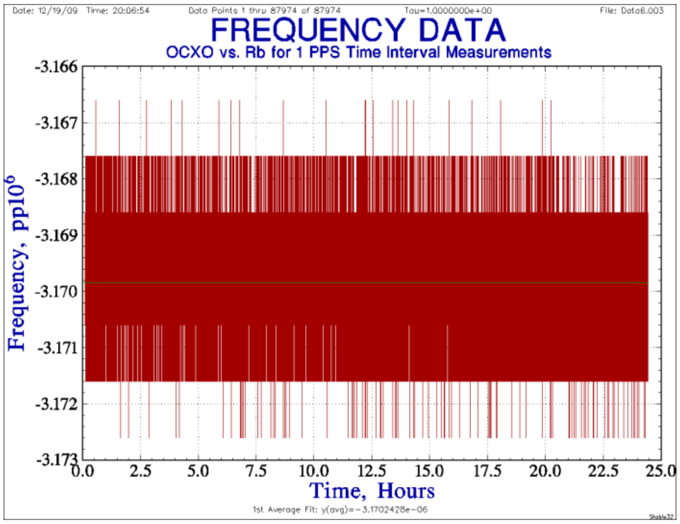

Figure 4. Frequency Data Plot

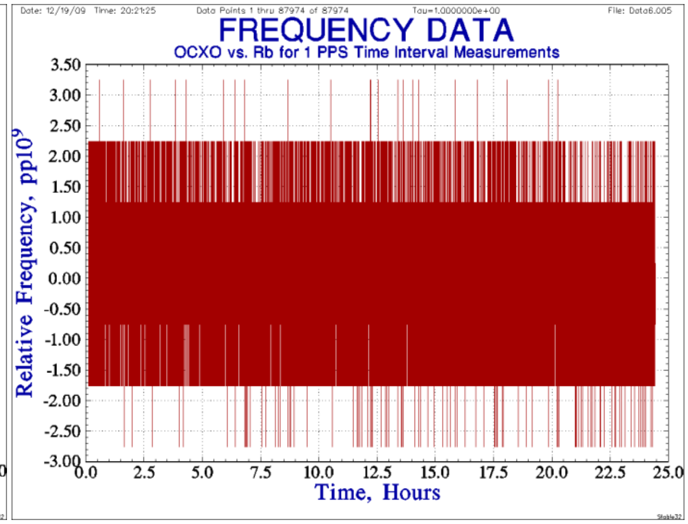

Figure 5. Relative Frequency Data Plot

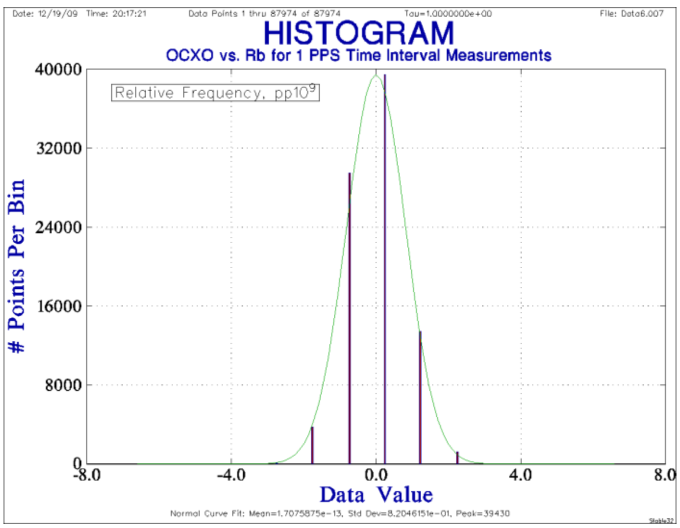

Figure 6. Histogram of Relative Frequency Data

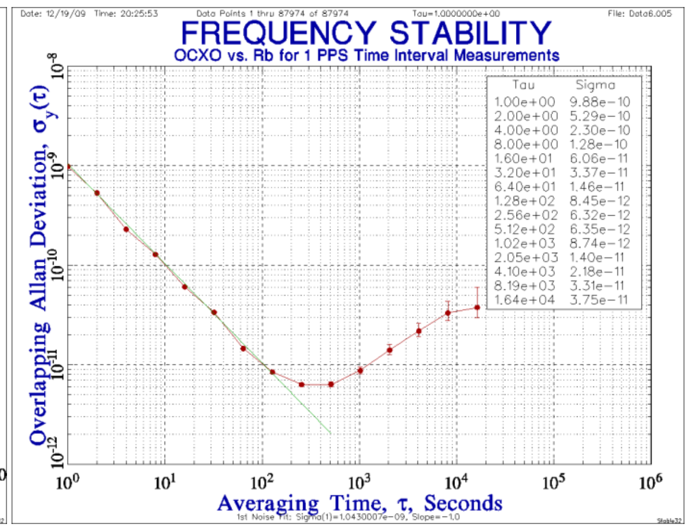

Figure 7. Stability Plot

Because of the short-term quantization noise, it is advisable to average these measurements by a factor or at least 100 in order to better see the longer-term behavior of the oscillator, as shown in Figure 8. This oscillator appears to have a drift on the order of $\approx -2.7\times10^{-10}$ per day, and the lurch toward the end of the record is probably due to a thermal change.

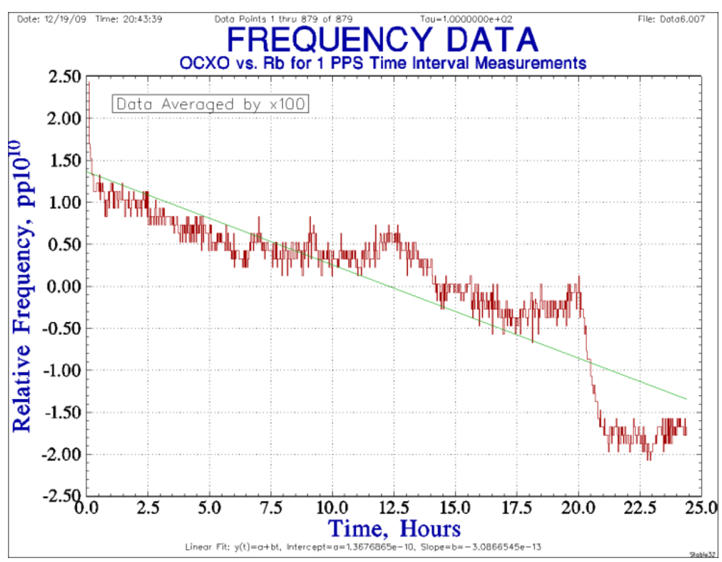

Figure 8. Frequency Data Plot

The PICTIC 1 PPS Clock Measuring System

The PICTIC 1 PPS clock measuring system comprises two 10 MHz to 1 PPS dividers as described above and an interpolating PICTIC time interval counter combined with a 10 MHz to 50 MHz clock multiplier, an RS-232 to USB converter, and two 50 Ω 1 PPS output buffers, as shown in the block diagram of Figure 9 and the photographs of Figures 10 and 11. It accomplishes the same type of clock measurement as described above with better resolution and without the need for a laboratory time interval counter instrument and associated GPIB interface. It also includes a custom Microsoft Windows® program to control the system and capture the data.

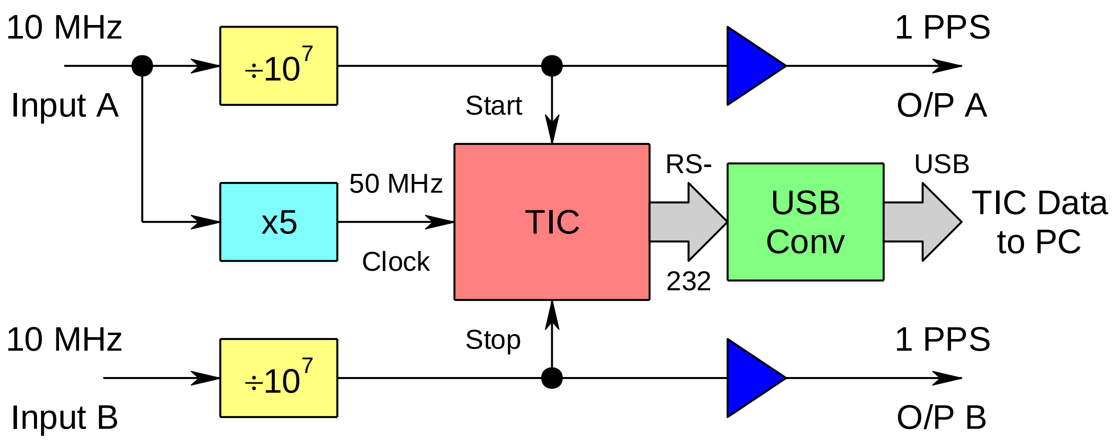

Figure 9. Block Diagram of 1 PPS PICTIC Clock Measuring System

Figure 10. Front View

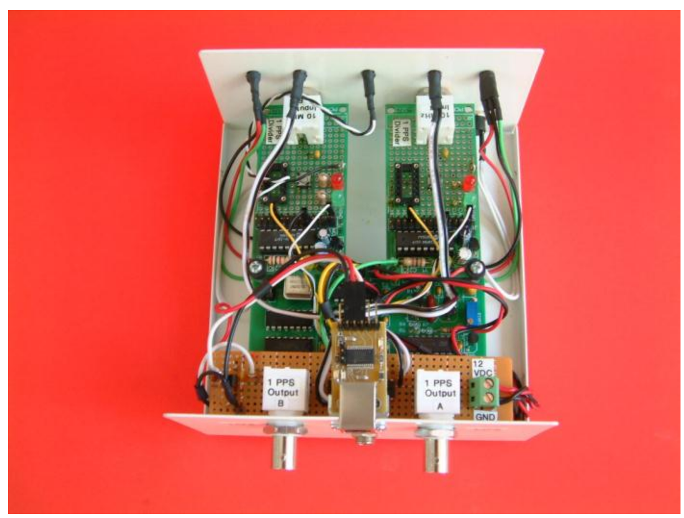

Figure 11. Interior View

Photographs of 1 PPS PICTIC Clock Measuring System

System Components

This 1 PPS clock measuring system employs two elegant components based on Microchip PIC microcontrollers. The 10 MHz to 1 PPS divider (see above) was developed by Tom Van Baak and is described in Reference [1]. Two of them are implemented here on small PICProto boards (see [2]) along with LMV7219 comparators to convert the 10 MHz sinewave input into a clock signal. The PICTIC time interval counter with its analog interpolator was developed by Richard McCorkle and is fully described in

Reference [6]. It is supplemented with a x5 clock multiplier using a 50 MHz bandpass filter and another LMV7219 comparator, a COMPSys FD232RB RS-232 to USB converter (see [7]) and two 50 Ω 1 PPS output drivers. These components are packaged in a 5” W x 3” H x 6” D aluminum box, and a custom PICTICComm Microsoft Windows ® program was written to support system operation, data capture and Stable32 analysis. The main screen of the PICTICComm program is shown in Figure 12. It includes provisions for automatically removing sawtooth phase spillovers. The PICTIC firmware was slightly modified for this application by adding a new @@Dz command to clear all display items. The 50 MHz clock provides the PICTIC system with a basic resolution of 20 nanoseconds, while its 400-count analog interpolator increases the overall resolution to 50 picoseconds.

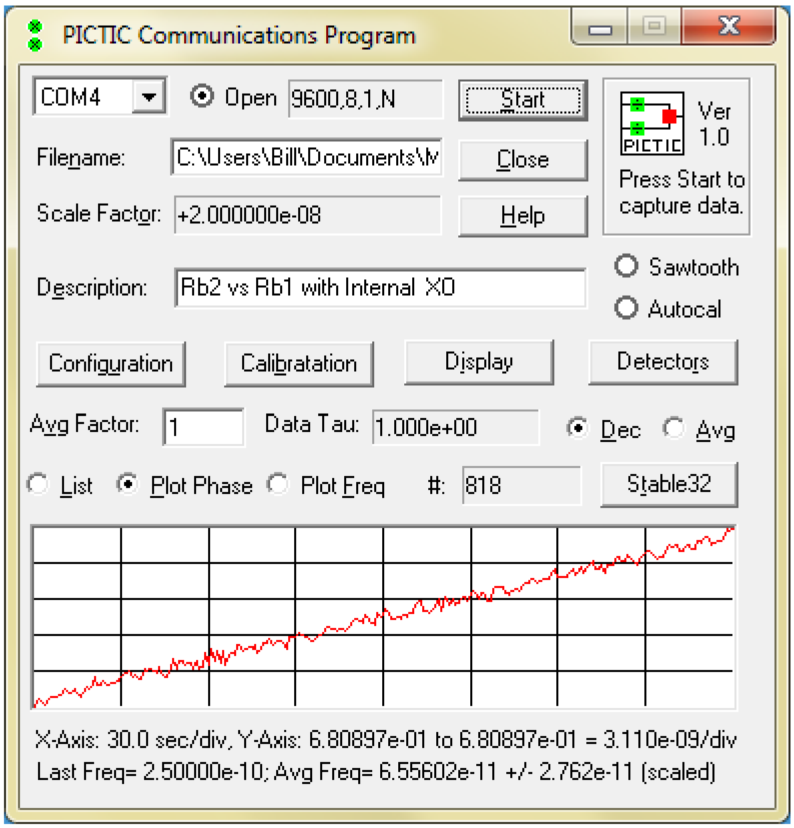

Figure 12. PICTICComm Main Screen

● Noise Test

A coherent noise test of the complete system was conducted by driving both inputs and the TIC clock from the same rubidium oscillator. Figures 13-16 show plots of the resulting phase, frequency, stability and frequency histograms. The relative phase data plot of Figure 13 shows quantization at the 50 ps system resolution, and a noise level an order-of-magnitude higher (≈ 500 ps peak). There is little or no evidence of environmental sensitivity, drift or wandering while exposed to air conditioner cycling. The PICTIC readings agree exactly with those of the external high-resolution laboratory time interval counter. The frequency plot of Figure 14 shows similar results, with a 1-second scatter of about $1x10^{-9}$ peak-to-peak and no appreciable frequency offset wandering or drift, and only slight periodic cycling. The stability plot of Figure 15 shows a 1-second Allan deviation of about $3x10^{-10}$ with a slope of τ^{-1} slope corresponding to a combination of white and flicker PM noise. The frequency histogram of Figure 16 shows the data quantization and a normal distribution. The stability plot shows signs of periodic ripple.

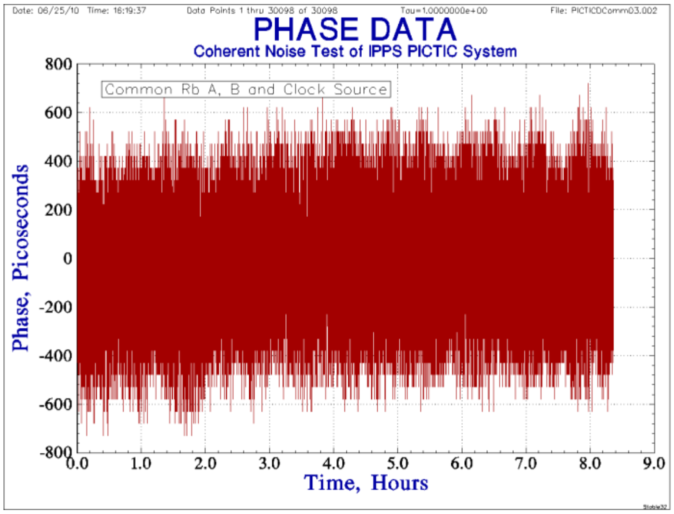

Figure 13. Coherent Phase Data Plot

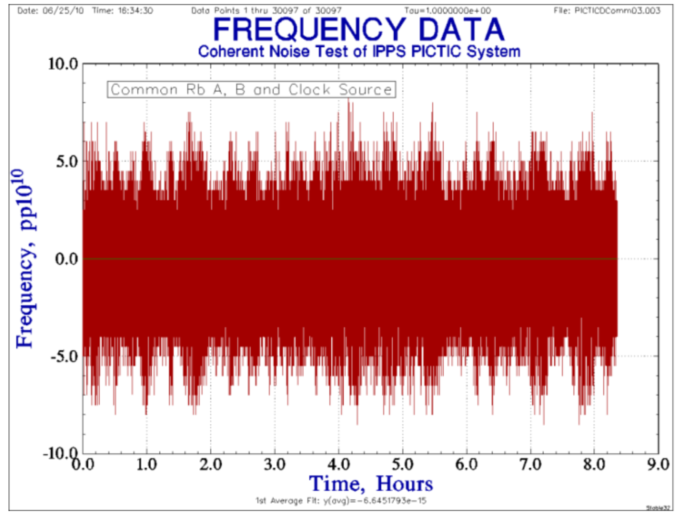

Figure 14. Coherent Frequency Data Plot

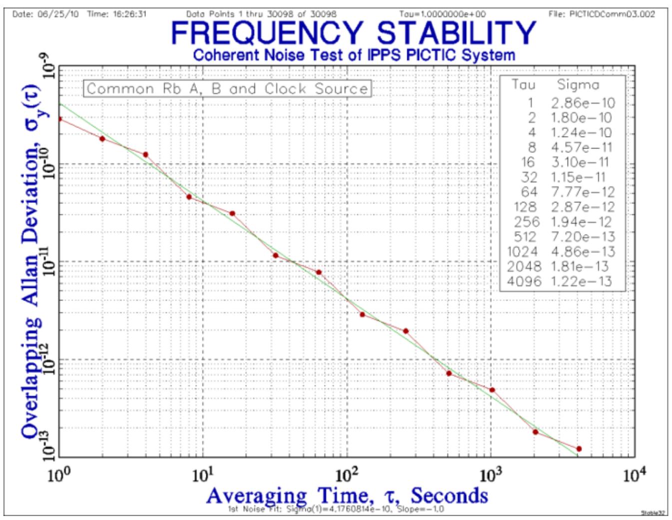

Figure 15. Coherent Stability Plot

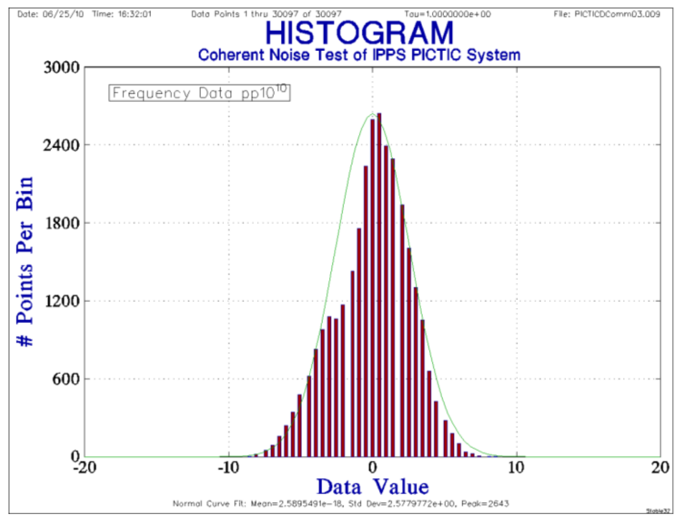

Figure 16. Coherent Frequency Histogram

1 PPS PICTIC System Coherent Noise Test Results

● Other Tests

Somewhat lower noise was obtained by reconfiguring the 1 PPS PICTIC clock measuring system to process measurements at a 10 PPS rate, supported with a higher 57600 baud serial communications rate. The 10 PPS measurement rate was obtained by simply selecting the 10 Hz PIC divider outputs, and the higher baud rate was obtained by a simple PICTIC firmware change. By using that arrangement, along with phase data averaging by a factor of 10, provided a 1-second noise level of about 1×10^{-10}, consistent with an improvement by the square root of the averaging factor. The phase record had peak excursions of about ±4 50 ps interpolator counts, the resulting histogram, all-tau stability, power spectral density and autocorrelation plots were all quite clean, and a frequency offset of a few $pp10^{13}$ could be measured in several minutes. Averaging is a form of integration that decreases the α of the noise process by 2, so the white PM noise ($\alpha = 2$) is changed to random walk PM noise ($\alpha = 0$), which is the same as white FM noise. The slope of the log-log sigma-tau stability plot will be changed from -1 (white PM) to -1/2 (white FM) in the vicinity of the measurement interval, and will revert to -1 at larger averaging factors (longer τ). Thus, while phase averaging can reduce the noise floor, it can also be a source of confusion when working at or near the noise floor, and it is generally not recommended.

Lower noise was also obtained with phase averaging of the 1 PPS data by the same factor of 10, which provided an extrapolated 1-second white PM ADEV of about 6×10^{-11}, as shown in Figure 17. The same setup using phase decimation by 10 had an extrapolated 1-second ADEV about x3 larger, 1.8×10^{-10}.

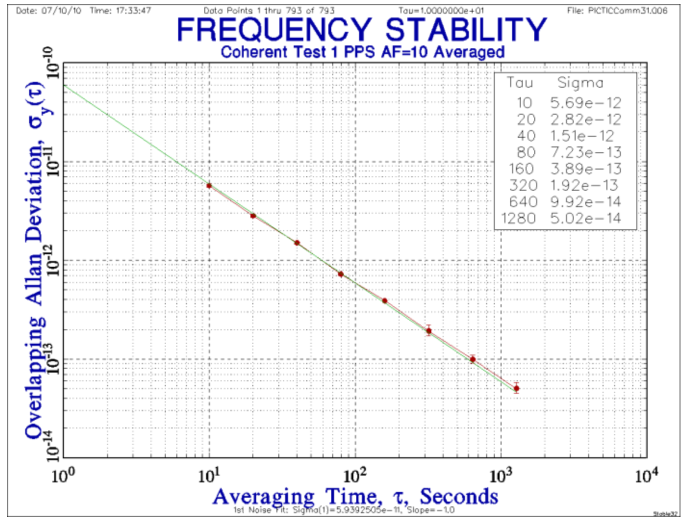

Figure 17. 1 PPS AF=10 Averaged Stability Plot

An inexpensive multichannel clock measuring system could be built with a set of 1 PPS dividers and either a single or multiple TICs to measure ovenized crystal oscillators or commercial rubidium frequency standards. Short-term stability measurements would require multiple TICs, but a single multiplexed TIC would suffice for collecting aging data. In either case, the phase of each source would be observed continuously by the dividers.

● Conclusion

The PICTIC noise lies between the quantization levels of its counter and interpolator, providing a low-cost alternative to a laboratory time interval counter, and is suitable for evaluating the stability of medium-performance clocks and oscillators.

● References

The following references apply to the 1PPS clock measuring systems:

1. T. Van Baak , 10 MHz to 1 PPS Divider.
2. MicroEngineering Labs, Inc., PICProto Boards.
3. Prologic, LLC, GPIB-USB Controller.
4. U. Bangert, EZGPIB, A GPIB, RS232 and TCP/IP Data Acquisition Tool.
5. Hamilton Technical Services, Stable32.
6. R. McCorkle, PICTIC Time Interval Counter.
7. COMPSys, FD232RB RS-232 to USB Converter.

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